Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P6459 Total Pages 2

First Named Inventor or Application Identifier Chien Chiang

Express Mail Label No. EL034430503US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)
2. X Specification (Total Pages 25)
   (preferred arrangement set forth below)
   - Cover Sheet
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 6)
4. X Oath or Declaration/Power of Attorney (Total Pages 4)
   a. X Unsigned
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. __ Incorporation By Reference (useable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. __ Microfiche Computer Program (Appendix)
7. __ Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. ___ Computer Readable Copy
   b. ___ Paper Copy (identical to computer copy)
   c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
    _____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
    b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. X Other: Certificate of Mailing (1 page in duplicate)

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____

(Insert Customer No. or Attach Bar Code Label here)

or

X Correspondence Address Below

NAME Gregory D. Caldwell, Reg. No. 39,926

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (503) 684-6200 FAX (503) 684-3245

Express Mail Label: EL034430503US

PTO/SB/17(10/96)
Approved for use through 09/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL

EXPRESS MAIL NO. EL034430503US

Complete if Known:
Application No. _____
Filing Date November 13, 1998
First Named Inventor Chien Chiang
Group Art Unit _____
Examiner Name _____
Attorney Docket No. 42390.P6459

METHOD OF PAYMENT (check one)

1. [ ] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

   Deposit Account Number 02-2666
   Deposit Account Name _____

   [X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

   [ ] **Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance, 37 CFR 1.131(b)**

2. X **Payment Enclosed**
   X **Check**
   _____ **Money Order**
   _____ **Other**

FEE CALCULATION (fees effective 10/01/97)

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility application filing fee	790.00
106	330	206	165	Design application filing fee	
107	540	207	270	Plant filling fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional application filing fee	
				SUBTOTAL (1)	$ 790.00

2. CLAIMS

			Extra		Fee from below		Fee Paid
Total Claims	29	– 20 =	9	X	22.00	=	198.00
Independent Claims	7	– 3 =	4	X	82.00	=	328.00
Multiple Dependent Claims				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
103	22	203	11	Claims in excess of twenty	198.00
102	82	202	41	Independent claims in excess of 3	328.00
104	270	204	135	Multiple dependent claim	
109	82	209	41	Reissue independent claims over original patent	
110	22	210	11	Reissue claims in excess of 20 and over original patent	
				SUBTOTAL (02)	$ 526.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	400	216	200	Extension for response within second month	
117	950	217	475	Extension for response within third month	
118	1,510	218	755	Extension for response within fourth month	
128	2,060	228	1,030	Extension for response within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,320	241	660	Petition to revive unintentionally abandoned application	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (see 37 CFR 1.129(a))	
Other fee (specify)					
Other fee (specify)					

SUBTOTAL (3) $ 0.00

*Reduced by Basic Filing Fee Paid

TOTAL AMOUNT OF PAYMENT ($)

$ 1316.00

SUBMITTED BY:

Typed or Printed Name: Gregory D. Caldwell

Signature _____ Date 11/12/98

Reg. Number 39,926 Deposit Account User ID _____ (complete if applicable)

PTO/SB/17 (10-96)
Approved for use through 09/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

P6459 PATENT

IN-PLANE ON-CHIP DECOUPLING CAPACITORS AND METHOD FOR MAKING SAME

Inventors: Chien Chiang
David B. Fraser

"Express Mail" mailing label number EL034430503US

"Express Mail" mailing label number EL034430503US
Date of Deposit November 13, 1998
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231
Mary E. Varian 11.13.98
Signature Date

IN-PLANE ON-CHIP DECOUPLING CAPACITORS AND METHOD FOR MAKING SAME

Inventors: Chien Chiang
David B. Fraser

Background of the Invention

Field of the Invention

The present invention relates generally to microelectronic structures and fabrication methods, and more particularly to in-plane decoupling capacitor structures and methods of making the same.

Background

Advances in semiconductor manufacturing technology have led to the development of integrated circuits having multiple levels, of interconnect. In such an integrated circuit, patterned conductive material on one interconnect level is electrically insulated from patterned conductive material on another interconnect level by films of material such as silicon dioxide. These patterned conductive materials are also referred to as interconnect lines. The spaced apart interconnect lines on each interconnect level are typically provided with insulating material therebetween The interconnect lines on each interconnect level are typically substantially co-planar. Connections between the conductive material at the various interconnect levels are made by forming openings in the insulating layers and providing an electrically conductive structure such that the patterned conductive material from different interconnect levels are brought into electrical contact with each other. These structures are often referred to as contacts or vias.

A consequence of having many interconnect lines separated by an insulating layer is the formation of undesired capacitors. The parasitic

capacitance between patterned conductive material, or more simply, interconnects, separated by insulating material on microelectronic devices contributes to effects such as RC delay, power dissipation, and capacitively coupled signals, also known as cross-talk. In view of the adverse effects of parasitic capacitance on the performance of integrated circuits, it is desirable to reduce the capacitance between interconnect lines. One way to reduce the unwanted capacitance between the interconnects is to use an insulating material with a lower dielectric constant.

Unlike parasitic capacitance between interconnect lines, which adversely affects circuit performance, decoupling capacitance is used to make circuits more robust in the presence of power supply noise. Decoupling capacitors are typically formed between power supply nodes. In this way, the rail-to-rail voltage across a circuit is protected to some degree from noise-induced voltage excursions in the power rails. Decoupling capacitors are often formed external to an integrated circuit, or may even be incorporated into the packaging of an integrated circuit.

What is needed is a structure that provides on-chip relatively high valued decoupling capacitors between power supply nodes, while providing low capacitance between interconnect lines that are used to carry signals. What is further needed are methods of making such a structure.

Summary of the Invention

Briefly, an interconnect structure for microelectronic devices includes a plurality of patterned, spaced apart, substantially co-planar, conductive lines, a first portion of the plurality of conductive lines having a first intralayer dielectric of a first dielectric constant therebetween, and second portion of the plurality of conductive lines having a second intralayer dielectric of a second dielectric constant therebetween.

Brief Description of the Drawings

Fig. 1 is a schematic cross-section of a patterned mask layer over a high dielectric constant material, which is formed over an insulating layer.

Fig. 2 is a schematic cross-section showing the high dielectric constant material of Fig. 1, after trenches have been etched, the trenches lined with a barrier layer, and a layer of conductive material formed thereover.

Fig. 3 is a schematic cross-section showing the structure of Fig. 2, after the conductive layer has been planarized.

Fig. 4 is a schematic cross-section showing the structure of Fig. 3, after a masking layer has been patterned and a portion of the intralayer dielectric material has been removed.

Fig. 5 is a schematic cross-section showing the structure of Fig. 4, after the masking layer has been removed and a low dielectric constant material has been deposited thereon.

Fig. 6 is a schematic cross-section showing the structure, in accordance with the present invention, of Fig. 5 after further processing to planarize the low dielectric constant material.

Fig. 7 is a schematic cross-section showing a plurality of patterned interconnect lines formed o an insulating substrate.

Fig. 8 is a schematic cross-section showing the structure of Fig. 7 with a first dielectric material disposed over its surface.

Fig. 9 is a schematic cross-section showing the structure of Fig. 8, after the first dielectric material has been planarized and a masking layer has been patterned over the surface.

Fig. 10 is a schematic cross-section showing the structure of Fig. 9, after the first dielectric material not covered by the patterned masking layer has been removed, and the masking layer has been removed.

Fig. 11 is a schematic cross-section showing the structure of Fig. 10, after a second dielectric material is disposed over its surface.

Fig. 12 is a schematic cross-section showing the structure, in accordance with the present invention, of Fig. 11 after further processing to planarize the second dielectric material.

Fig. 13 is a schematic cross-section showing a patterned masking layer over a layer having patterned interconnect lines and a first intralayer dielectric of a first dielectric constant.

Fig. 14 is a schematic cross-section showing the structure of Fig. 13, after processing operations remove the unmasked portions of the first intralayer dielectric, remove the patterned masking layer, and dispose over its surface a second dielectric material of a second dielectric constant.

Fig. 15 is a schematic cross-section showing the structure of Fig. 14, after the second dielectric material is planarized.

Fig. 16 is a schematic cross-section showing the structure of Fig. 15, after further operations mask the existing interconnect lines, and form additional interconnect lines by damascene processing in the area of the second dielectric.

Fig. 17 is a schematic cross-section showing a patterned masking layer over a first dielectric material which itself is disposed over a substrate.

Fig. 18 is a schematic cross-section showing the structure of Fig. 17, after an exposed portion of the first dielectric material is removed, and the patterned masking layer is removed.

Fig. 19 is a schematic cross-section showing the structure of Fig. 18, after a second dielectric material is disposed over its surface.

Fig. 20 is a schematic cross-section showing the structure of Fig. 19, after the second dielectric material is planarized.

Fig. 21 is a schematic cross-section showing the structure of Fig. 20, after interconnect lines are formed by a damascene process in both the areas having the first dielectric material and the areas having the second dielectric material.

Detailed Description

Terminology

The terms, chip, integrated circuit, monolithic device, semiconductor device, and microelectronic device, are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnect or simply metal. Metal lines, such as aluminum (Al), copper (Cu) an alloy of Al and Cu, an alloy of Al, Cu and silicon (Si), an alloy of Cu and magnesium (Mg), or an alloy of Cu and niobium (Nb), are conductors that provide signal paths for coupling or interconnecting, electrical circuitry. Conductors other than metal are available in microelectronic devices. Materials such as doped polysilicon, doped single-crystal silicon (often referred to simply as diffusion, regardless of whether such doping is achieved by thermal diffusion or ion implantation), titanium (Ti), tantalum (Ta), tantalum nitride (TaN), tungsten (W), nickel (Ni), molybdenum (Mo), and refractory metal silicides are examples of other conductors.

The terms contact and via, both refer to structures for electrical connection of conductors from different interconnect levels. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure contact and via refer to the completed structure.

The expression, low dielectric constant material, refers to materials having a lower dielectric constant than oxides of silicon. For example, organic polymers, nanofoams, silicon based insulators containing organic polymers, and fluorine containing oxides of silicon have lower dielectric constants than silicon dioxide.

The letter k, is often used to refer to dielectric constant. Similarly, the terms high-k, and low-k, are used in this field to refer to high dielectric constant and low dielectric constant respectively.

The term intralayer dielectric as used in this field is understood to refer to the dielectric material disposed between interconnect lines on a given interconnect level. That is, an intralayer dielectric is found between adjacent interconnect lines, rather than vertically above or below those interconnect lines.

The term vertical, as used herein, means substantially perpendicular to the surface of a substrate.

Overview

Interconnect lines on integrated circuits are generally used for the distribution of power and signals. Those skilled in the art will recognize that integrated circuit power supply nodes typically include large amounts of interconnect. These power supply interconnect lines are needed to distribute power throughout the integrated circuit.

Capacitance between interconnect lines in integrated circuits is well-known to be a function of the distance, i.e., separation, between the lines, the dielectric constant of the material between the lines, and the area over which the lines face each other. In fact, for many simple modeling purposes, the parallel plate capacitor is used to model the capacitance between interconnect lines.

Conventionally, the interconnect lines on a given level of chip interconnect have the same dielectric material disposed in between them. This results from conventional manufacturing processes, and means that all these interconnect lines have a material with a given dielectric constant between them.

Reducing the capacitance between interconnect lines by increasing the distance between the lines tends to result in a larger, and thus more expensive, chip. Therefore, in order to reduce the undesired effects of parasitic capacitance

between signal-carrying interconnect lines, manufacturers have increasingly sought to use low dielectric constant material between interconnect lines. Unfortunately, in conventional processes, reducing the dielectric constant of the material disposed between interconnect lines, not only reduces parasitic capacitance, it also reduces decoupling capacitance.

In some instances it is desirable to increase on-chip capacitance between power supply nodes so as to increase the decoupling capacitance that in turn helps to provide noise immunity for the individual circuits on a chip. At the same time, it is generally desirable to reduce the capacitance between signal-carrying interconnect lines. As is known in this field, reducing the parasitic capacitance between signal carrying lines results in higher speed operation and lower power consumption.

Embodiments of the present invention provide integrated circuits having increased localized decoupling capacitance between power supply nodes, without unduly adding to the parasitic capacitance between signal nodes. More particularly, embodiments of the present invention provide, on a given interconnect level, high dielectric constant material as an intralayer dielectric between power supply nodes and low dielectric constant material as an intralayer dielectric between signal nodes. In this way, in-plane decoupling between power supply nodes is improved, while maintaining the advantages of low parasitic capacitance between signal carrying interconnect lines.

Embodiments of the present invention may be particularly useful for integrated circuits that use copper as the primary material for interconnect lines. Since copper has a lower resistivity than other conductive materials that have traditionally been used for interconnect lines, it is possible to achieve traditional values of sheet resistance while using thinner interconnect lines. Thinner interconnect lines are desirable for reducing parasitic capacitance between signal-carrying interconnect lines, but this is disadvantageous in that such an

arrangement reduces the decoupling capacitance between adjacent power supply interconnect lines.

A first illustrative embodiment of the present invention that incorporates damascene processing, is described in conjunction with Figs. 1-6, and a second illustrative embodiment of the present invention that incorporates a subtractive metal process, is described in conjunction with Figs. 7-12. Two further illustrative embodiments of the present invention, both of which incorporate damascene processing, are described in conjunction with Figs. 13-16, and Figs. 17-21 respectively.

Referring now to Figs. 1-6, a method, in accordance with the present invention, of forming interconnect on a microelectronic device wherein a first portion of the interconnect lines have a high dielectric constant material formed therebetween and a second portion of the interconnect lines have a low dielectric constant material formed therebetween, is described.

Fig.1 shows a cross-sectional view of a portion of a wafer and more particularly shows an insulating substrate **102** over which a first dielectric layer **104** is formed. A masking material is then deposited onto the surface and patterned to form patterned masking layer **106**. Masking materials and photolithography techniques for patterning masking materials are well-known in this field.

Subsequent to the formation of patterned masking layer **106**, an etching operation is performed such that trenches are formed in first dielectric layer **104** as shown in Fig. 2. Fig. 2 also shows that an operation is performed to produce liners **108** which cover the inner surfaces of the trenches. In the illustrative embodiment, liners **108** are typically formed by depositing a thin layer of titanium nitride over the surface of the wafer, including the inner surfaces of the trenches, and then removing that portion of the titanium nitride that is outside the inner surfaces of the trenches. The titanium nitride removal process is typically a chemical mechanical polishing operation. Subsequent to the formation of liners

108, a conductive material **110**, such as, for example, copper, is deposited over the surface of the wafer.

Fig. 3 shows a cross-sectional view of the wafer shown in Fig. 2, after a planarization operation has been performed. Those skilled in the art and having the benefit of this disclosure will recognize that patterned interconnect lines **110a**, **110b**, **110c**, result from planarizing conductive material **110** such that the conductive material remains in the trenches, which include liners **108**, and is substantially removed from the surface of first dielectric layer **104**. Typically, such planarization is achieved by chemical mechanical polishing.

Referring to Fig. 4, a masking layer **112** is patterned over the surface of the wafer such that a portion of the intralayer dielectric material **104** is exposed. After masking layer **112** is patterned, an etching operation is performed such that the exposed dielectric **104** is removed. After the etching operation, masking layer **112** is removed.

As can be seen in Fig. 5, a layer of a second dielectric material **114** is deposited onto the surface of the wafer. The dielectric constant of second dielectric material **114** is different from the dielectric constant of first dielectric material **104**.

Fig. 6 shows a cross-sectional view of the structure of Fig. 5, subsequent to a planarization operation. More particularly, Fig. 6 shows interconnect lines **110a** and **110b** with first dielectric material **104** therebetween and interconnect lines **110b** and **110c** with second dielectric material **114** therebetween. In the illustrative embodiment of the present invention shown in Fig. 6, the dielectric constant of dielectric material **104** is greater than the dielectric constant of dielectric material **114**. Consequently, the capacitance between interconnect lines **110a** and **110b**, is greater than the capacitance between interconnect lines **110b** and **110c**, for a given area and spacing. Alternatively, it can be said that the unit capacitance between interconnect lines **110a** and **110b**, is greater than the unit capacitance between interconnect lines **110b** and **110c**.

Alternatively, the dielectric constant of dielectric material **104** may be less than the dielectric constant of dielectric material **114**. In this alternative embodiment, the unit capacitance between interconnect lines **110a** and **110b**, is less than the unit capacitance between interconnect lines **110b** and **110c**.

A further alternative method of forming interconnect on a microelectronic device wherein a first portion of the interconnect lines have a high dielectric constant material formed therebetween and a second portion of the interconnect lines have a low dielectric constant material formed therebetween, in accordance with the present invention, is described below in conjunction with Figs. 7-12.

Fig. 7 shows a cross-sectional view of a portion of a wafer and more particularly shows an insulating substrate **202** over which interconnect lines **204a**, **204b**, **204c**, and **204d** are formed. Interconnect lines **204a**, **204b**, **204c**, and **204d** are made of conductive material such as, for example, aluminum, aluminum alloys, or stacks of various metals, such as, for example aluminum and titanium. The present invention is not limited to any particular conductive material.

Referring to Fig. 8, a first dielectric material **206** is deposited onto the surface of the wafer.

Subsequently, first dielectric material **206** is planarized, as shown in Fig. 9. Planarization is typically, but not required to be, achieved by chemical mechanical polishing. A masking material is then deposited and patterned to form masking layer **208**. Masking layer **208** is patterned in such a way that a first portion of intralayer dielectric material **206** is exposed, and a second portion of intralayer dielectric material **206** is covered.

Referring to Figs. 9 and 10, it can be seen that the exposed first portion of intralayer dielectric material **206** is removed by etching. Masking layer **208** is then removed. As shown in Fig. 10, the structure includes an insulating substrate **202** with conductive interconnect lines **204a**, **204b**, **204c**, and **204d**

formed thereon, dielectric material **206** between interconnect lines **204b**, **204c**, and **204d**, and gaps **205** surrounding interconnect line **204a**.

As shown in Fig. 11, a layer of a second dielectric material **208** is deposited over the surface of the wafer. Second dielectric material **208** has a dielectric constant that is different from the dielectric constant of first dielectric material **206**.

A structure as shown in the cross-sectional view of Fig. 12, results from the planarization of the structure shown in Fig. 11. Typically, such a planarization is achieved by chemical mechanical polishing. As can be seen in Fig. 12, interconnect lines **204a** and **204b** have second dielectric material **208** therebetween and interconnect lines **204b** and **204c** as well as interconnect lines **204c** and **204d** have first dielectric material **206** therebetween. In the structure of the illustrative embodiment of the present invention shown in Fig. 12, the dielectric constant of dielectric material **208** is greater than the dielectric constant of dielectric material **206**. Consequently, the capacitance between interconnect lines **204a** and **204b**, is greater than the capacitance between interconnect lines **204b** and **204c**, for a given area and spacing. Alternatively, it can be said that the unit capacitance between interconnect lines **204a** and **204b**, is greater than the unit capacitance between interconnect lines **204b** and **204c**.

Alternatively, the dielectric constant of dielectric material **208** may be less than the dielectric constant of dielectric material **206**. In this alternative embodiment, the unit capacitance between interconnect lines **204a** and **204b**, is less than the unit capacitance between interconnect lines **204b** and **204c**.

In one typical embodiment of the present invention, a pair of interconnect lines that are coupled to a positive power supply node, and a ground node, respectively, are placed adjacent, but spaced apart from each other, on a particular interconnect level. Simultaneously, a pair of interconnect lines that are coupled to a first signal node, and a second signal node, respectively, are placed adjacent, but spaced apart from each other, on the same interconnect level with

the power supply interconnect lines. In this embodiment of the present invention, a first dielectric material is disposed between the power supply interconnect lines and a second dielectric material is disposed between the signal interconnect lines. More particularly, the first dielectric material, i.e., the dielectric material between the power supply interconnect lines has a higher dielectric constant than the second dielectric material.

Referring to Figs. 13-16, an alternative embodiment of the present invention is described. In this embodiment interconnect lines are formed by a damascene process in a first dielectric material. These interconnect lines and the immediately surrounding dielectric material are then masked, and the remainder of the dielectric material is removed. A second dielectric material is then deposited and planarized. Subsequently, additional interconnect lines are formed by a damascene process in the area of the second dielectric material.

Fig. 13 is a schematic cross-section of a substrate **302** having patterned interconnect lines **308** and a first intralayer dielectric **304** of a first dielectric constant formed thereon. In this illustrative embodiment, first intralayer dielectric **304** comprises a high-k material. A patterned masking layer **310**, which overlies interconnect lines **308** and a portion of first intralayer dielectric **304**, is formed by conventional methods. In this illustrative embodiment, a liner **306** is disposed between interconnect lines **308** and first intralayer dielectric **304**. Those skilled in the art will appreciate that a liner is sometimes used with interconnect lines so as to prevent undesirable interactions between the conductive material of the interconnect lines and the dielectric material that otherwise surrounds the interconnect lines.

Fig. 14 is a schematic cross-section showing the structure of Fig. 13, after processing operations remove the unmasked portions of first intralayer dielectric **304**, remove patterned masking layer **310**, and dispose over its surface a second intralayer dielectric **312** of a second dielectric constant. In the illustrative embodiment second intralayer dielectric **312** comprises a low-k material.

Referring to Fig. 15, it can be seen that a planarization operation has been performed on second intralayer dielectric **312** such that a substantially planar surface is achieved. Planarization operations are well known in this field and are often achieved by chemical-mechanical polishing.

A structure in accordance with the present invention is shown in schematic cross-section in Fig. 16. More particularly, Fig. 16 shows the structure of Fig. 15, after further operations mask existing interconnect lines **308** in an area **316**, and form additional interconnect lines by damascene processing in an area **314** of second intralayer dielectric **312**. Various well-known photolithographic, etching, deposition, and polishing methods can be used to protect existing interconnect lines **308**, etch trenches in second intralayer dielectric **312**, deposit a conductive material and polish back that conductive material to form additional interconnect lines **308** in area **314**.

Those skilled in the art and having the benefit of this disclosure will recognize that the process and structure described above in connection with Figs. 13-16, can be rearranged such that intralayer dielectric **304** is a low-k dielectric, and that intralayer dielectric **312** is a high-k dielectric. In this case, interconnect lines **308** in region **314** would preferably be power lines, and interconnect lines **308** in region **316** would preferably be signal lines.

Similarly, those skilled in the art and having the benefit of this disclosure will recognize that the process and structure described above in connection with Figs. 13-16, can be altered such that a hardmask layer is formed over first intralayer dielectric **304** and interconnect lines **308** prior to the formation of masking layer **310**. Such a hardmask layer may be formed of a material such as, but not limited to, silicon nitride. This type of hardmask layer can provide protection of the underlying layers during processing operations.

Referring to Figs. 17-21, a further alternative embodiment of the present invention is described. In this embodiment, a first dielectric layer is formed on a substrate. A masking layer is then patterned to define an area of the first

dielectric that is to be removed. This area is then etched, the masking layer is removed, and a second dielectric material is deposited and planarized. At this point, the substrate has a planarized dielectric layer wherein the dielectric layer has two different materials with different dielectric constants. A damascene process is then used to form interconnect lines.

Fig. 17 is a schematic cross-section showing a patterned masking layer **406** over a first dielectric material **404**, which, in turn, is disposed over a substrate **402**. In the illustrative embodiment, substrate **402** is a wafer with various electrical components, interconnections, and insulating regions formed therein. First dielectric **406** is any suitable material with a dielectric constant greater than or equal to the dielectric constant of silicon dioxide. Barium strontium titinate (BST) is one example of a high-k material.

Referring to Fig. 18, it can be seen that both an exposed portion of first dielectric material **404**, and patterned masking layer **406** have been removed. Well-known photolithographic and etching operations can be used to form the patterned dielectric structure shown in Fig. 18.

As can be seen in Fig. 19, a second dielectric material **408** is disposed over the surface of substrate **402** and patterned dielectric layer **404**. In this illustrative embodiment of the present invention, second dielectric material **408** has a dielectric constant that is different from that of first dielectric material **404**.

Fig. 20 shows the structure of Fig. 19, after second dielectric material **408** is planarized. Various methods of planarization are well known in this field and the present invention is not restricted in any way to a particular planarization method. Typically, chemical-mechanical polishing is used to achieve a planarized surface. While planarization of the second dielectric material is preferred, those skilled in the art and having the benefit of this disclosure will recognize that depending on the thickness of the various dielectric layers and the degree of planarity with which they are formed, it may be possible to eliminate this particular planarization operation.

Fig. 21 is a schematic cross-section showing the structure of Fig. 20, after interconnect lines **412** are formed by a damascene process in both the areas having first dielectric **404** and the areas having second dielectric **408**. In this illustrative embodiment, a liner **410** is disposed between interconnect lines **412** and intralayer dielectrics **404**, **408**. Liner **410** may be formed of a material such as, but not limited to, titanium nitride. Those skilled in the art will appreciate that a liner is sometimes used with interconnect lines so as to prevent undesirable interactions between the conductive material of the interconnect lines and the dielectric material that otherwise surrounds the interconnect lines.

Several process flows have been described above, however each produces substantially the same structure. As can be seen by referring to the structures shown in Figs. 6, 12, 16, and 21, a structure in accordance with the present invention includes conductive lines on a particular interconnect level wherein a first set of lines have a first dielectric material of a first dielectric constant disposed between them, and a second set of lines have a second dielectric material of a second dielectric constant disposed between them. Typically, the power distribution interconnect lines have a high-k dielectric material therebetween, while the signal carrying interconnect lines have a low-k dielectric disposed therebetween. In this way, fine tuning of in-plane inter-line capacitance can be achieved. Structures embodying the present invention may provide increased decoupling between power distribution interconnect lines while simultaneously providing reduced parasitic capacitance between signal carrying interconnect lines.

Conclusion

Embodiments of the present invention provide low dielectric constant insulation between a first set of interconnects, and high dielectric constant insulation between a second set of interconnects on integrated circuits, where the first and second set of interconnects are on the same interconnect level.

An advantage of embodiments of the present invention is that capacitance between signal interconnect lines is reduced while capacitance between power supply nodes is increased. By selectively defining co-planar high-k and low-k intralayer dielectric regions, integrated circuit layout designs can reduce parasitic capacitance between signal lines while increasing the decoupling capacitance between nodes such as power and ground.

The present invention may be implemented with various changes and substitutions to the embodiments described and illustrated herein. For example, the present invention may be implemented without the need to etch away portions of the first intralayer dielectric material. In such an embodiment a masking material would block the formation and/or placement of the first dielectric material between a first portion of the plurality of interconnect lines on the integrated circuit. After formation of the first intralayer dielectric, the masking material would be removed and the second intralayer dielectric formed.

Those skilled in the art and having the benefit of this disclosure will recognize that embodiments of the present invention may have more than two varieties of intralayer dielectric materials. That is, multiple regions may be created on an integrated circuit wherein intralayer dielectrics are tailored for specific circuit design goals. It will be understood that the present invention is not limited to a particular number of intralayer dielectric zones where the various zones have intralayer dielectric structures that provide different effective dielectric constants.

It will be readily understood by those skilled in the art that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated in order to explain the nature of this invention may be made without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A structure, comprising:

a plurality of patterned, spaced apart, substantially co-planar, conductive lines;

wherein a first portion of the plurality of conductive lines have a first dielectric of a first dielectric constant therebetween, and a second portion of the plurality of conductive lines have a second dielectric of a second dielectric constant therebetween.

2. The structure of Claim 1, wherein the first dielectric constant is less than the second dielectric constant.

3. The structure of Claim 2, wherein the conductive lines comprise a metal

4. The structure of Claim 3, wherein the metal is selected from the group consisting of aluminum, copper, alloys of aluminum, alloys of copper, titanium, tantalum, tungsten, and nickel.

5. The structure of Claim 2, wherein the first dielectric comprises an organic polymer.

6. The structure of Claim 2, wherein the first dielectric comprises a silicon based insulator containing an organic polymer.

7. The structure of Claim 2, wherein the first dielectric comprises a nanofoam.

8. The structure of Claim 2, wherein the first dielectric comprises a fluorine doped oxide of silicon.

9. The structure of Claim 2, wherein the second dielectric comprises a material having a dielectric constant greater than the dielectric constant of silicon dioxide.

10. The structure of Claim 2, wherein the second dielectric comprises barium strontium titinate.

11. The structure of Claim 2, wherein at least one of the first portion of the plurality of conductive lines is coupled to a first power supply node, and at least one of the first portion of the plurality of conductive lines is coupled to a second power supply node.

12. The structure of Claim 2, wherein at least one of the second portion of the plurality of conductive lines is coupled to a first signal node, and at least one of the second portion of the plurality of conductive lines is coupled to a second signal node.

13. An integrated circuit comprising:

a first and a second interconnect line, and a first dielectric material having a first dielectric constant disposed therebetween;

a third and a fourth interconnect line and a second dielectric material having a second dielectric constant disposed therebetween;

wherein the first and second interconnect lines are coupled to a first and a second power supply node respectively; the third and fourth interconnect lines are coupled to a first and a second signal node respectively; the first, second, third and fourth interconnect lines are on the same interconnect level, and the second dielectric constant is less than the first dielectric constant.

14. The integrated circuit of Claim 13, wherein the second dielectric material comprises an organic polymer.

15. The microelectronic structure of Claim 13, wherein the second dielectric material comprises a silicon based insulator containing an organic polymer.

16. The microelectronic structure of Claim 13, wherein the first dielectric material comprises barium strontium titinate.

17. A method of forming an interconnect structure, comprising:

forming a first layer of a first dielectric material on a substrate;

patterning the first layer;

depositing conductive material over the patterned first layer;

planarizing the conductive material such that a plurality of interconnect lines are formed;

forming a mask layer over the interconnect lines and patterned first layer;

patterning the mask layer such that a first portion of the interconnect lines and patterned first layer are covered, and a second portion of the interconnect lines and patterned first layer are uncovered;

removing the dielectric material from the uncovered portion;

removing the patterned mask layer; and

depositing a second layer of a second dielectric material.

18. The method of Claim 17, wherein the first dielectric material has a dielectric constant greater than a dielectric constant of the second dielectric material.

19. The method of Claim 17, wherein the first dielectric material has a dielectric constant less than a dielectric constant of the second dielectric material.

20. A method of forming an interconnect structure, comprising:

forming a first layer of a conductive material on a substrate;

forming interconnect lines from the conductive material;

depositing a first dielectric material over and between the interconnect lines;

forming a mask layer over the interconnect lines and first dielectric material;

patterning the mask layer such that a first portion of the interconnect lines and first dielectric material are covered, and a second portion of the interconnect lines and first dielectric material are uncovered;

removing the first dielectric material from the uncovered portion;

removing the patterned mask layer; and

depositing a second dielectric material.

21. The method of Claim 21, wherein the first dielectric material has a dielectric constant greater than a dielectric constant of the second dielectric material.

22. The method of Claim 21, wherein the first dielectric material has a dielectric constant less than a dielectric constant of the second dielectric material.

23. A method of making in-plane decoupling capacitors, comprising:

forming a first plurality of conductive lines on an insulating substrate, the first plurality of conductive lines having a first dielectric therebetween; and

forming a second plurality of conductive lines on the insulating substrate, the second plurality of conductive lines having a second dielectric therebetween;

wherein the first dielectric has a dielectric constant greater than a dielectric constant of the second dielectric.

24. A method of forming an interconnect structure, comprising:

forming, on a substrate, a first plurality of interconnect lines and a first intralayer dielectric disposed between the first plurality of interconnect lines;

removing a portion of the first intralayer dielectric;

forming a second intralayer dielectric on the substrate where the first intralayer dielectric was removed; and

forming a second plurality of interconnect lines in the second intralayer dielectric.

25. The method of Claim 24, wherein a dielectric constant of the first intralayer dielectric is different from a dielectric constant of the second intralayer dielectric.

26. The method of Claim 25, wherein forming the second plurality of interconnect lines comprises etching trenches in the second intralayer dielectric, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

27. A method of forming an interconnect structure, comprising:

forming a first dielectric layer on a substrate;

removing a portion of the first dielectric layer;

forming a second dielectric layer on the substrate where the portion of the first dielectric layer was removed; and

forming a plurality of interconnect lines in the first and second dielectric layers.

28. The method of Claim 27, wherein a dielectric constant of the first dielectric is different from a dielectric constant of the second dielectric.

29. The method of Claim 28, wherein forming the plurality of interconnect lines comprises etching trenches in the first and the second dielectrics, depositing a conductive material, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches.

ABSTRACT OF THE DISCLOSURE

An interconnect structure for microelectronic devices includes a plurality of patterned, spaced apart, substantially co-planar, conductive lines, a first portion of the plurality of conductive lines having a first intralayer dielectric of a first dielectric constant therebetween, and a second portion of the plurality of conductive lines having a second intralayer dielectric of a second dielectric constant therebetween. By providing in-plane selectability of dielectric constant, in-plane decoupling capacitance, as between power supply nodes, can be increased, while in-plane parasitic capacitance between signal lines can be reduced.

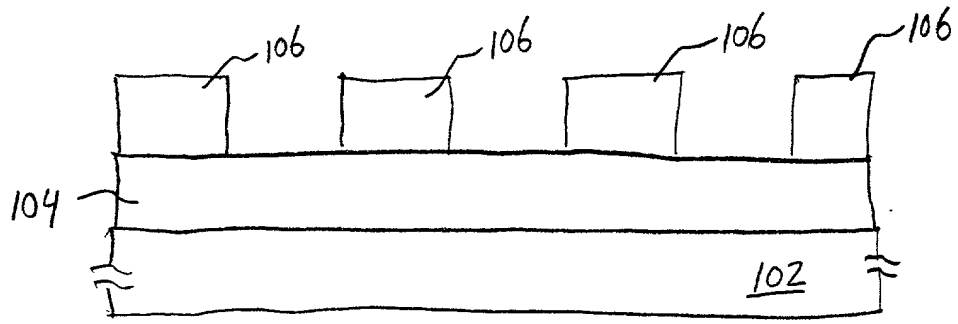

Fig. 1

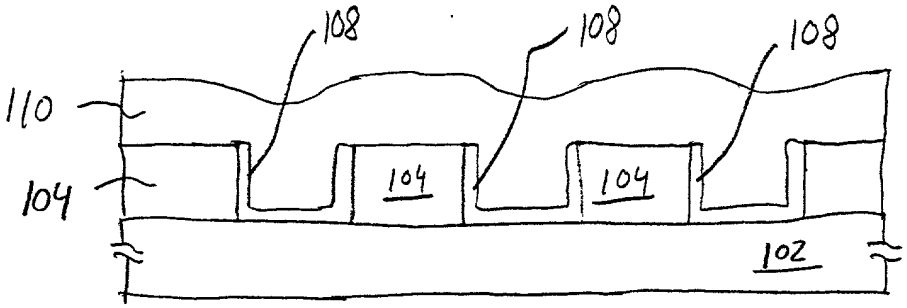

Fig. 2

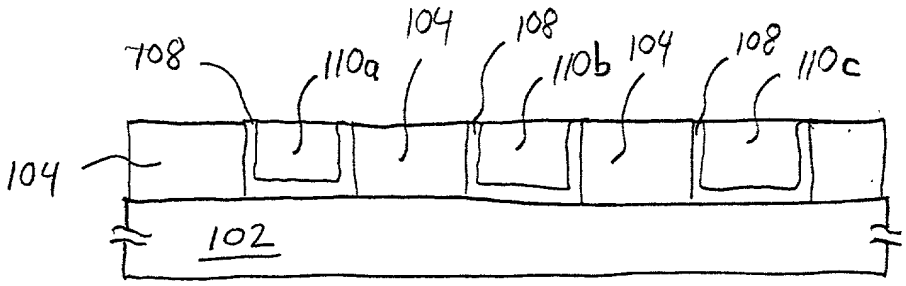

Fig. 3

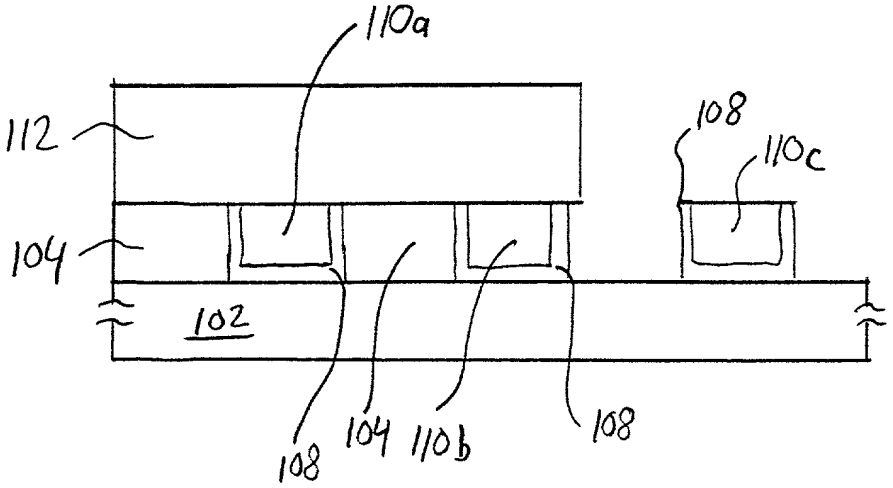

Fig. 4

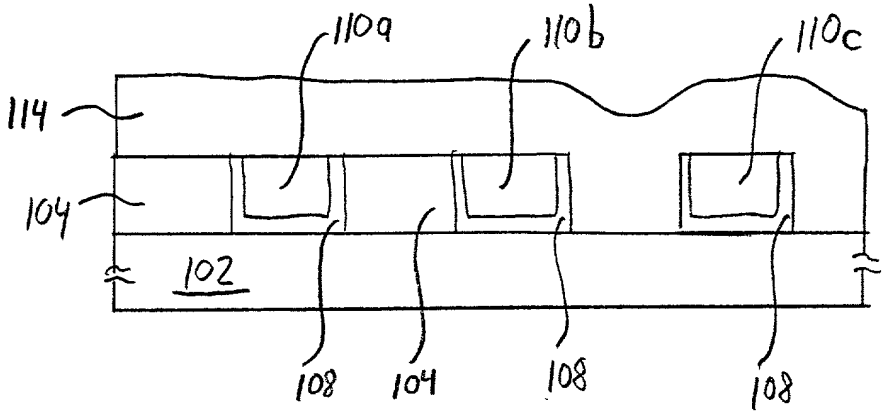

Fig. 5

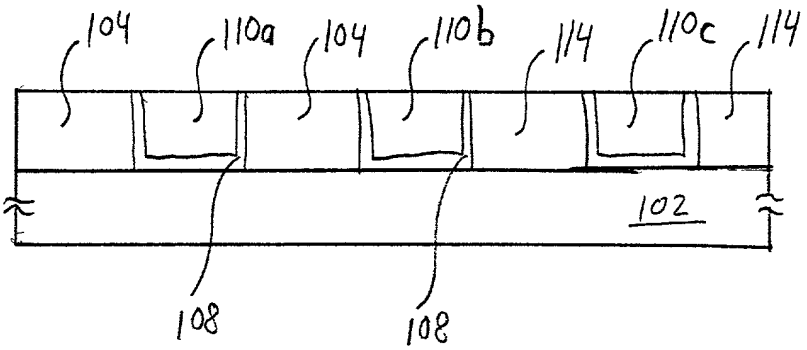

Fig. 6

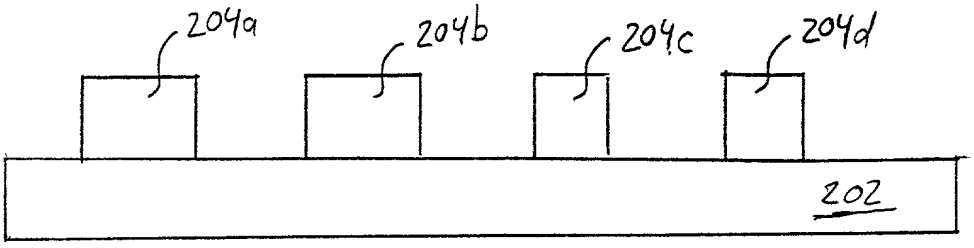

Fig. 7

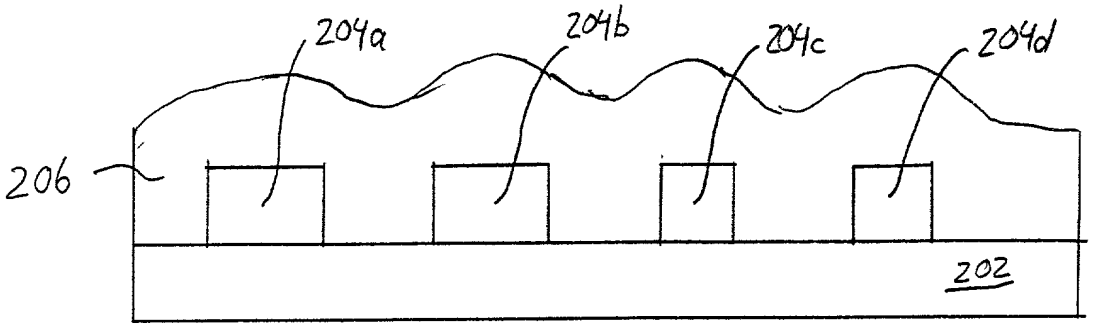

Fig. 8

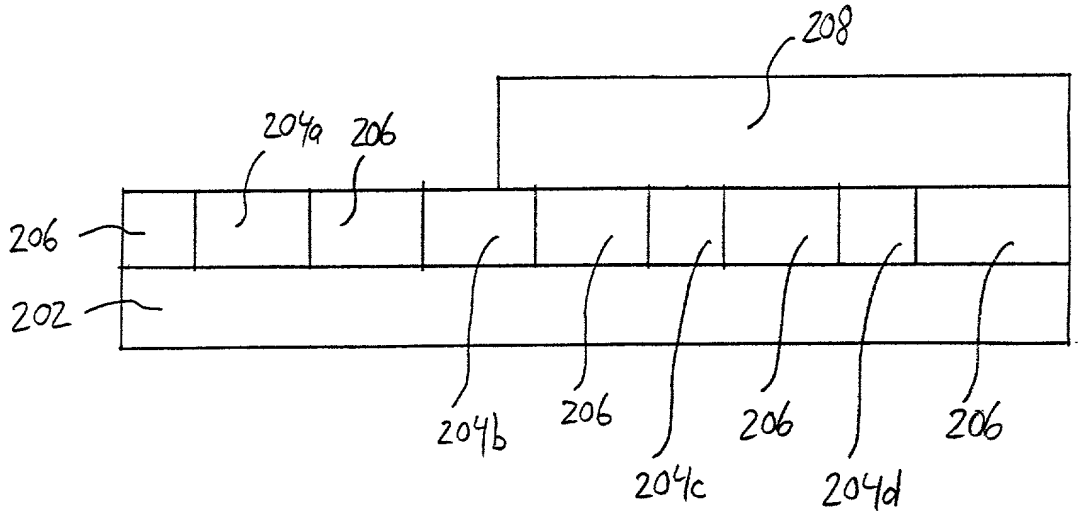

Fig. 9

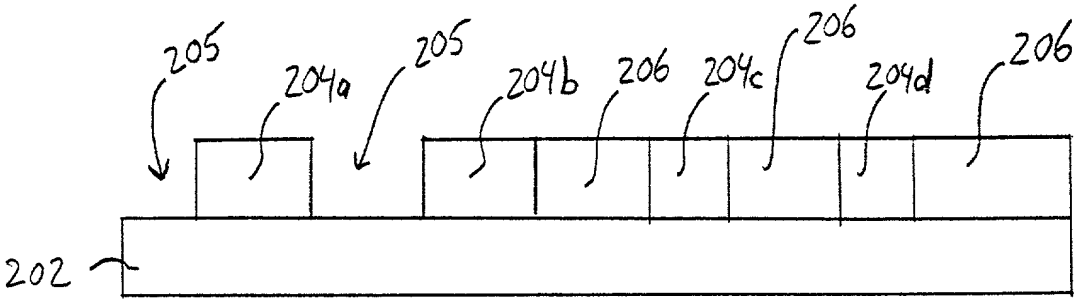

Fig. 10

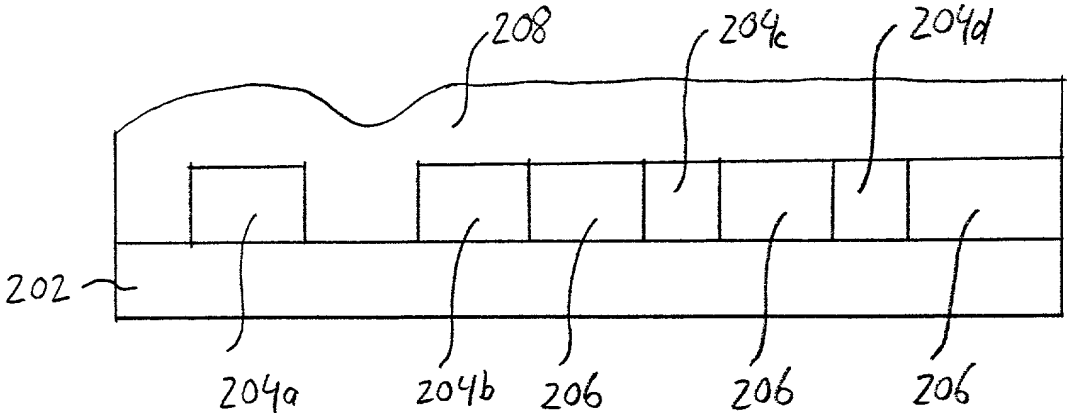

Fig. 11

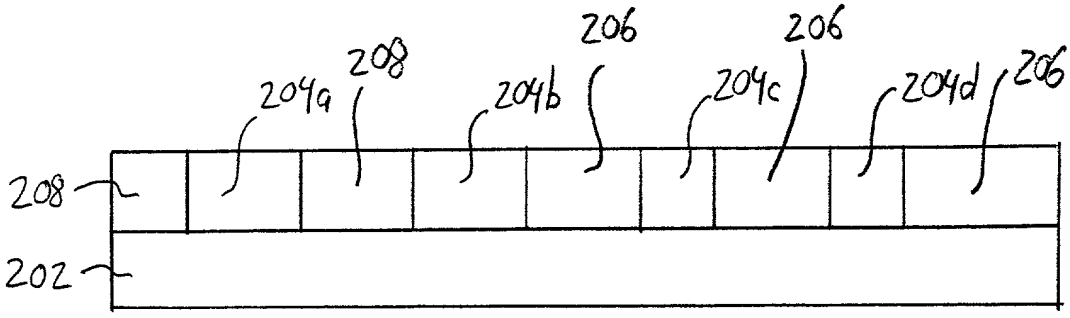

Fig. 12

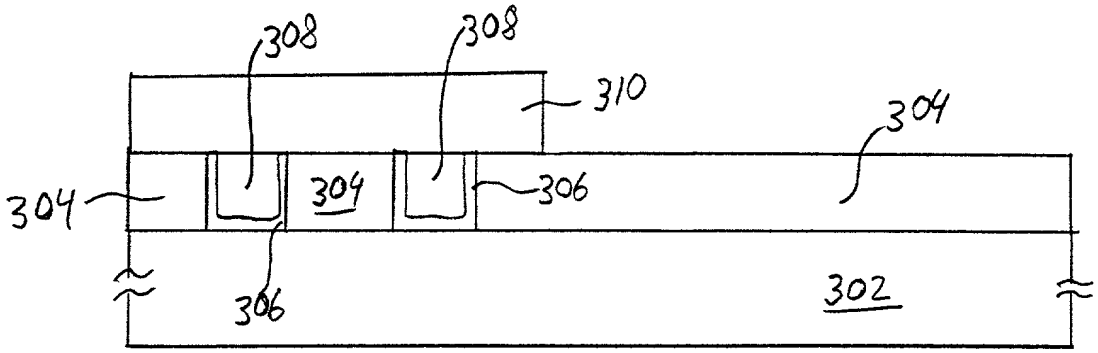

Fig. 13

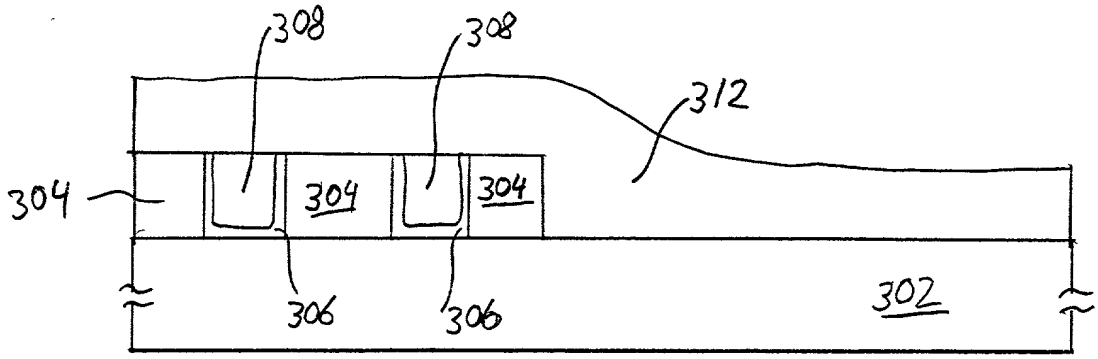

Fig. 14

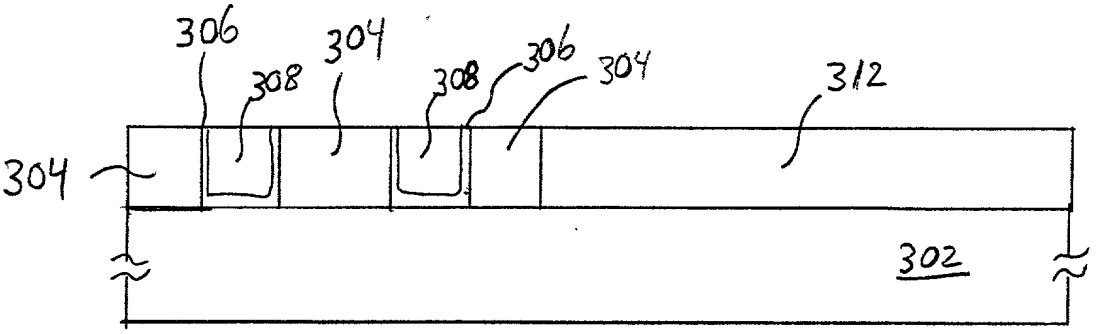

Fig. 15

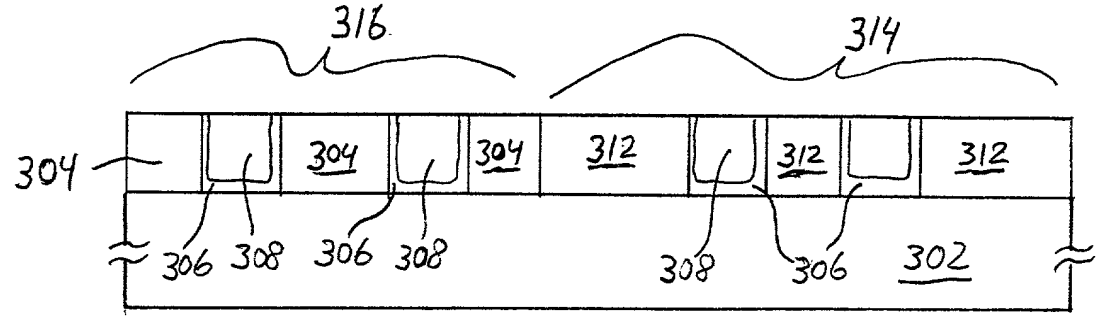

Fig. 16

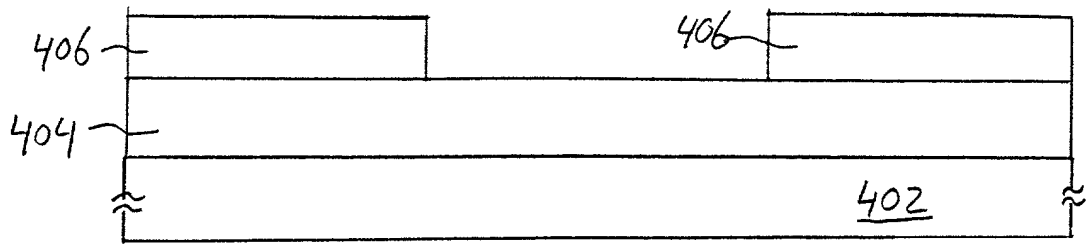

Fig. 17

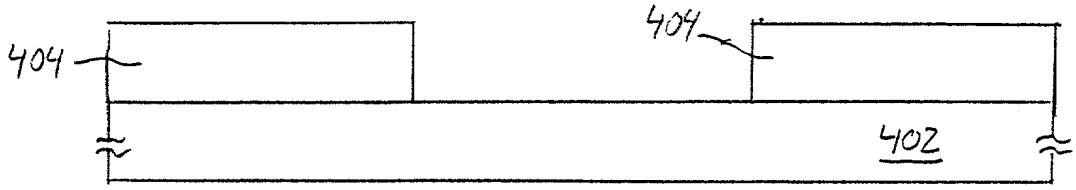

Fig. 18

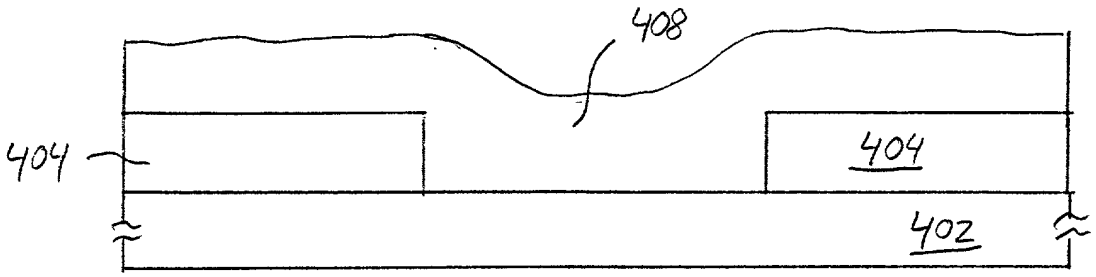

Fig. 19

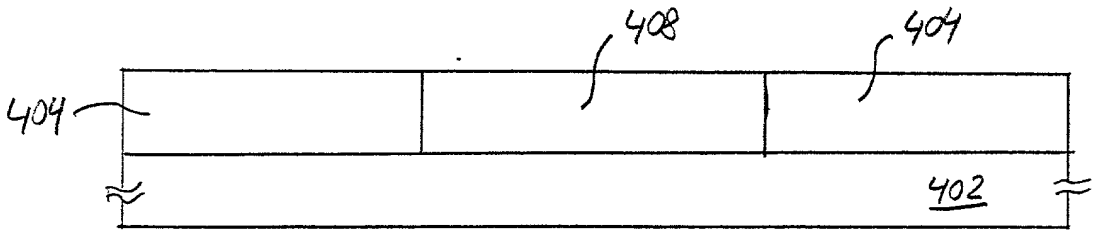

Fig. 20

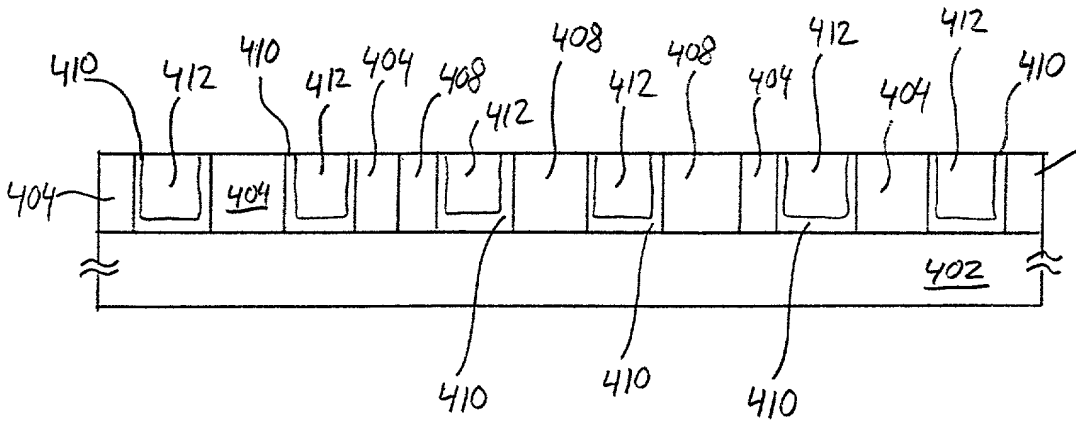

Fig. 21

Attorney's Docket No.: 42390.P6459 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

IN-PLANE ON-CHIP DECOUPLING CAPACITORS AND METHOD FOR MAKING SAME

the specification of which

__X__ is attached hereto.
_____ was filed on _____ As
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. P42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. P41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, P41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, 42,004; Thinh V. Nguyen, P42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, P42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. P42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. P43,237; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Jeffrey S. Draeger, Reg. No. 41,000; Thomas Raleigh Lane, Reg. No. P42,781; Calvin E. Wells, Reg. No. P43,256; and Alexander Ulysses Witkowski, Reg. No. P43,280; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Raymond J. Werner, Intel,
(Name of Attorney or Agent)
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Raymond J. Werner, Intel, (503)264-1421.

INTEL CORPORATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor CHIEN CHIANG

Inventor's Signature _____ Date _____

Residence Fremont,California (City, State) Citizenship United States (Country)

Post Office Address 45490 Concho Court
Fremont, California 94539

Full Name of Joint/Second Inventor DAVID B. FRASER

Inventor's Signature _____ Date _____

Residence Danville, California (City, State) Citizenship Canadian (Country)

Post Office Address 38 Cameron Court
Danville, California 94506